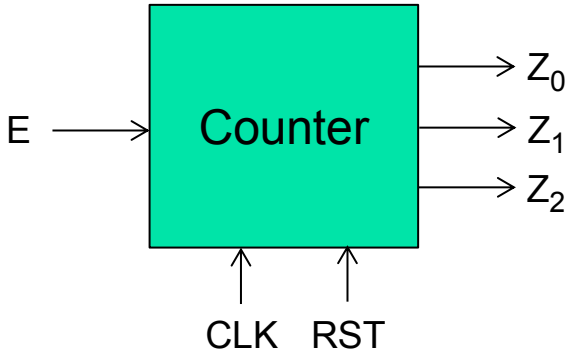
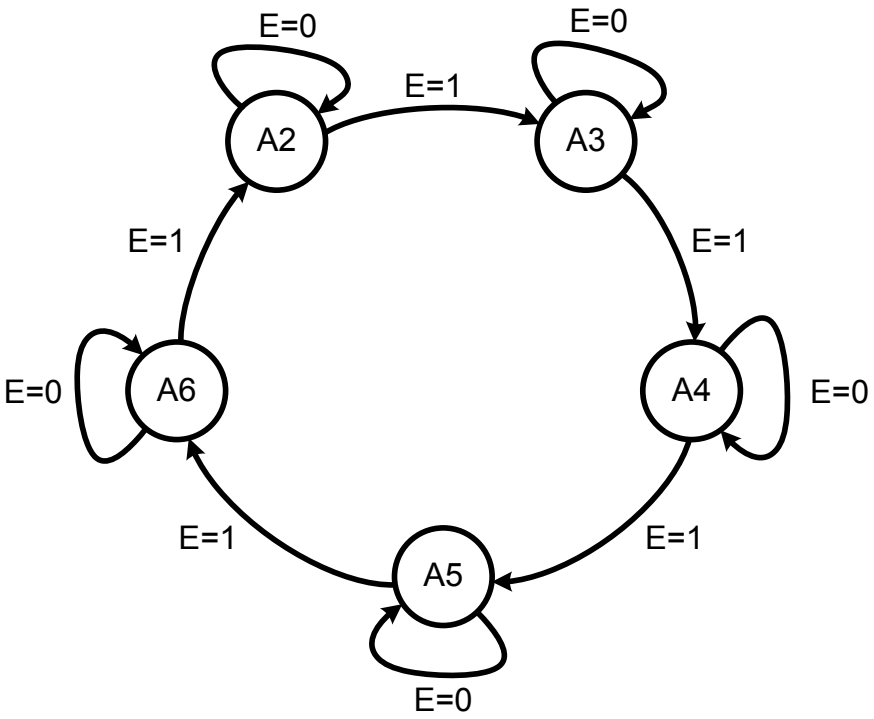
The Task

- Design a binary counter with enable signal (E):
  - The counter counts from 2 to 6.
  - It changes its value on every clock cycle (CLK) if E = '1'.
    If E = '0', the counter keeps its current value.
  - When the counter reaches value 6, it starts all over again from 2.
  - After reset (RST) the counter value is 2.
  - In the implementation use T-type flip-flops.



- Hint: First, derive the state diagram by using 5 states, i.e., one for every possible output value from 2 to 6.

State Diagram and State Table



Input E	Present State	Next State	Output Z
0	A2	A2	2
1	A2	A3	2
0	A3	A3	3
1	A3	A4	3
0	A4	A4	4
1	A4	A5	4
0	A5	A5	5
1	A5	A6	5
0	A6	A6	6
1	A6	A2	6

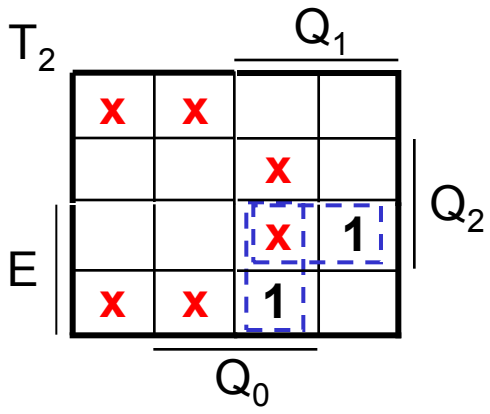
Encoded State Table

	Input	Present State			Next State			Output		
	E(t)	$Q_2(t)$	$Q_1(t)$	$Q_0(t)$	$Q_2(t+1)$	$Q_1(t+1)$	$Q_0(t+1)$	$Z_2(t)$	$Z_1(t)$	$Z_0(t)$
2	0	0	1	0	0	1	0	0	1	0
a	1	0	1	0	0	1	1	0	1	0
3	0	0	1	1	0	1	1	0	1	1
b	1	0	1	1	1	0	0	0	1	1
4	0	1	0	0	1	0	0	1	0	0
c	1	1	0	0	1	0	1	1	0	0
5	0	1	0	1	1	0	1	1	0	1
d	1	1	0	1	1	1	0	1	0	1
6	0	1	1	0	1	1	0	1	1	0
e	1	1	1	0	0	1	0	1	1	0

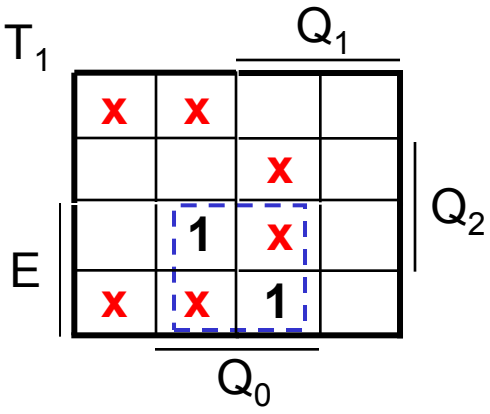
Ordered Encoded State Table

Input	Present State			Next State			FF inputs			Output		
E(t)	$Q_2(t)$	$Q_1(t)$	$Q_0(t)$	$Q_2(t+1)$	$Q_1(t+1)$	$Q_0(t+1)$	T_2	T_1	T_0	$Z_2(t)$	$Z_1(t)$	$Z_0(t)$
0	0	0	0	x	x	x	x	x	x	x	x	x
0	0	0	1	x	x	x	x	x	x	x	x	x
0	0	1	0	0	1	0	0	0	0	0	**1**	0
0	0	1	1	0	1	1	0	0	0	0	**1**	**1**
0	1	0	0	1	0	0	0	0	0	**1**	0	0
0	1	0	1	1	0	1	0	0	0	**1**	0	**1**
0	1	1	0	1	1	0	0	0	0	**1**	**1**	0
0	1	1	1	x	x	x	x	x	x	x	x	x
1	0	0	0	x	x	x	x	x	x	x	x	x
1	0	0	1	x	x	x	x	x	x	x	x	x
1	0	1	0	0	1	1	0	0	**1**	0	**1**	0
1	0	1	1	1	0	0	**1**	**1**	**1**	0	**1**	**1**
1	1	0	0	1	0	1	0	0	**1**	**1**	0	0
1	1	0	1	1	1	0	0	**1**	**1**	**1**	0	1
1	1	1	0	0	1	0	**1**	0	0	**1**	**1**	0
1	1	1	1	x	x	x	x	x	x	x	x	x

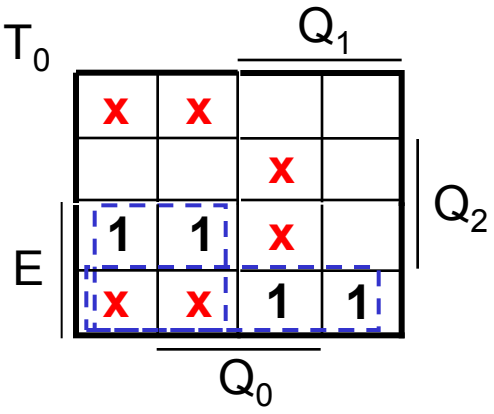
FFs Input and Counter Output Equations



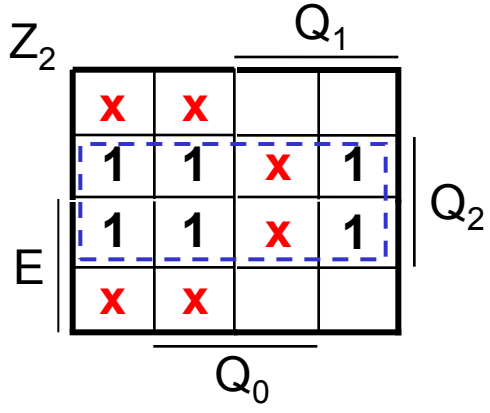
$T_2 = E \bullet Q_1 \bullet Q_0 + E \bullet Q_2 \bullet Q_1$



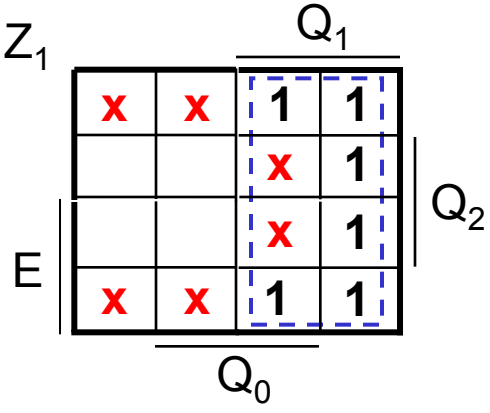
$T_1 = E \bullet Q_0$



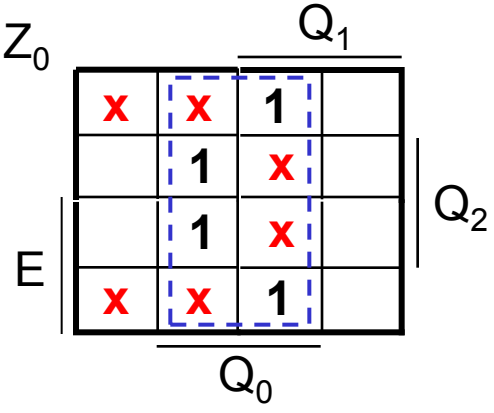
$T_0 = E \bullet Q1' + E \bullet Q_2'$



$Z_2 = Q_2$



$Z_1 = Q_1$



$Z_0 = Q_0$

Schematic of the Counter