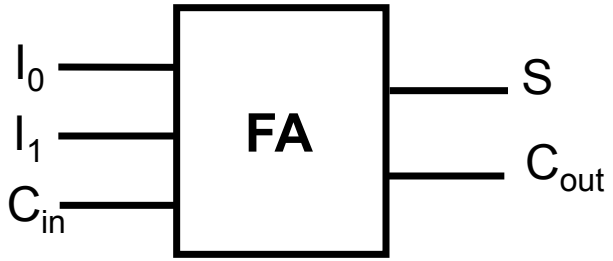
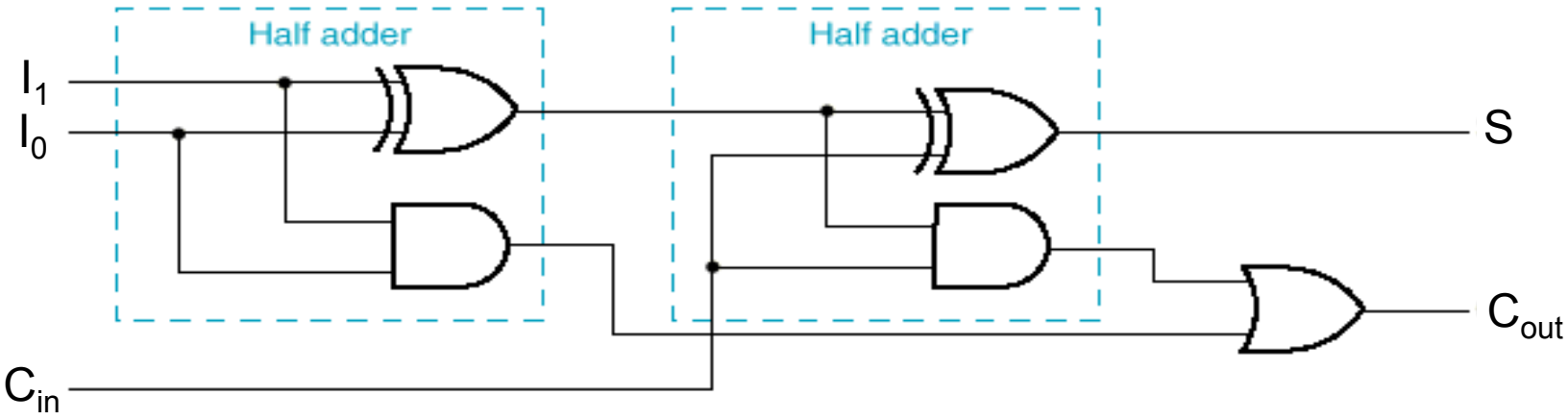
Task 1

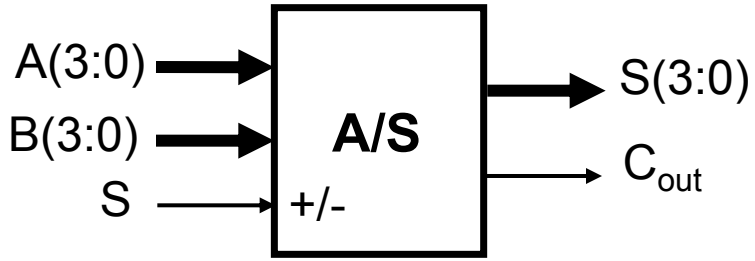
Design a Full Adder using 2 Half Adders.



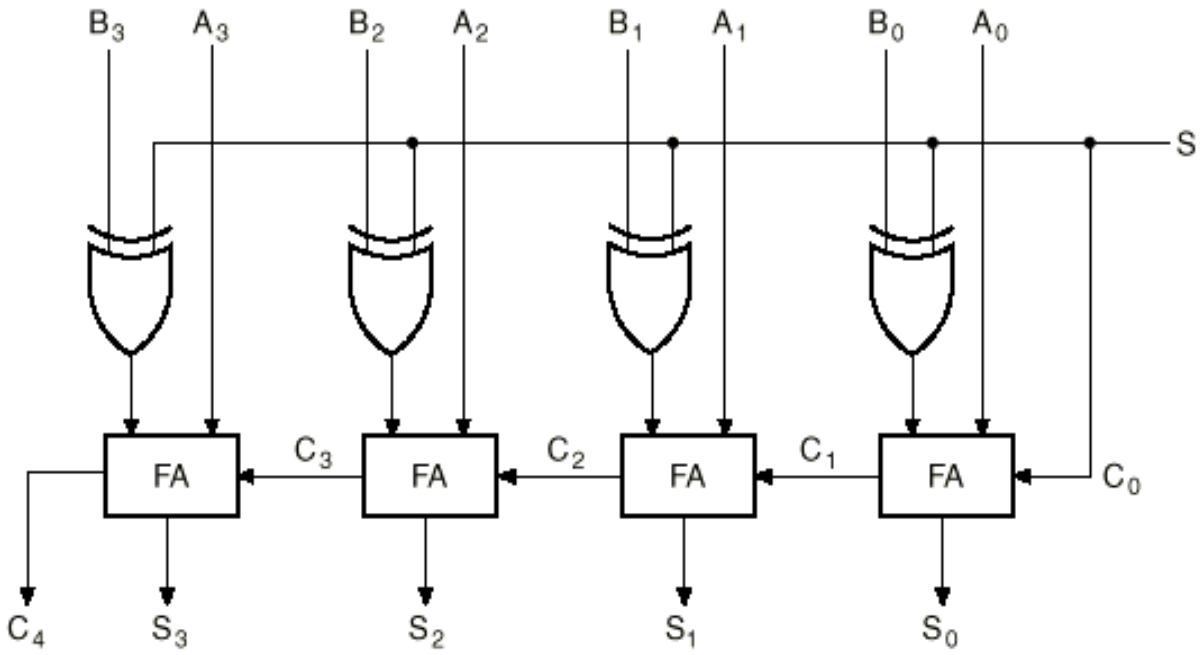


Task 2

Design 4-bit 2's complement Adder/Subtractor.



We will use 2's complement signed numbers.



S = 0 : "Addition"
S = 1 : "Subtraction"

Task 3

Using your Adder/Subtractor, show that:

	0 100	(+4)	
+	0 010	(+2)	
	0 110	(+6)	

	0 100	(+4)	
+	1 110	(-2)	
1	0 010	(+2)	

	1 100	(-4)	
+	0 010	(+2)	
	1 110	(-2)	

	1 100	(-4)	
+	1 110	(-2)	
1	1 010	(-6)	

	0 100	(+4)	
-	0 010	(+2)	
1	0 010	(+2)	

	0 100	(+4)	
-	1 110	(-2)	
	0 110	(+6)	

	1 100	(-4)	
-	0 010	(+2)	
1	1 010	(-6)	

	1 100	(-4)	
-	1 110	(-2)	
	1 110	(-2)	

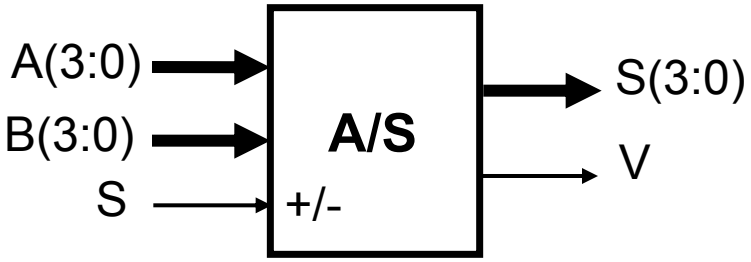
	0 110	(+6)	
+	0 100	(+4)	
	? ???	(??)	

	1 010	(-6)	
+	1 100	(-4)	
	? ???	(??)	

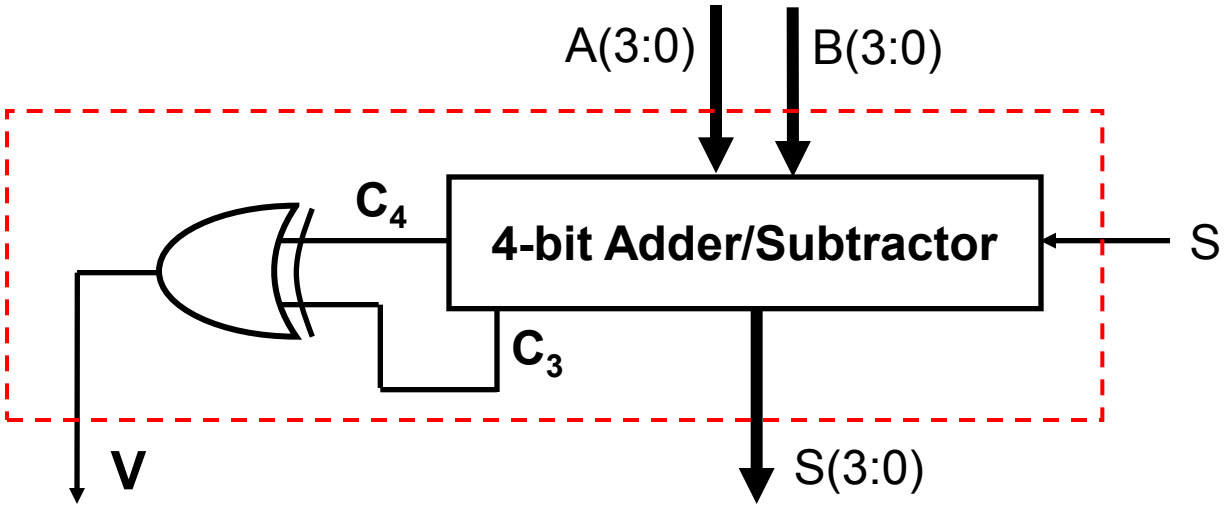
Your 4-bit Adder-Subtractor operates on **3-bit signed numbers.**
The **4-th bit** in the numbers is interpreted as the sign bit.

Task 4

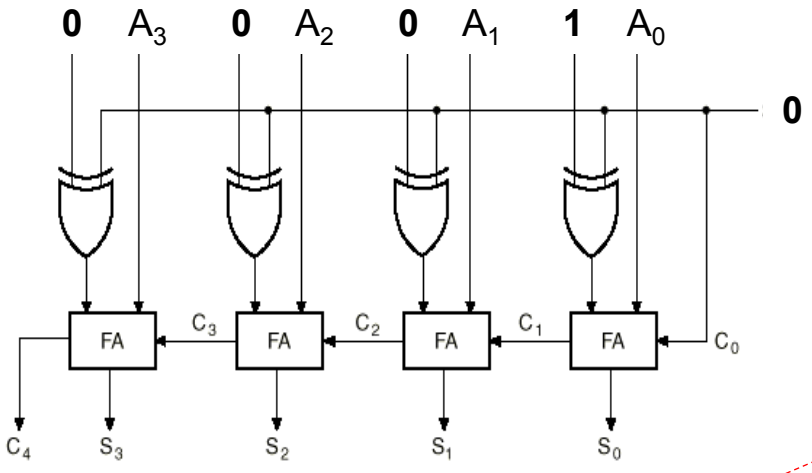
Design 4-bit Adder/Subtractor with Overflow Detection Logic.



- V = 1 indicates overflow condition when adding/subtracting signed-2's complement numbers.



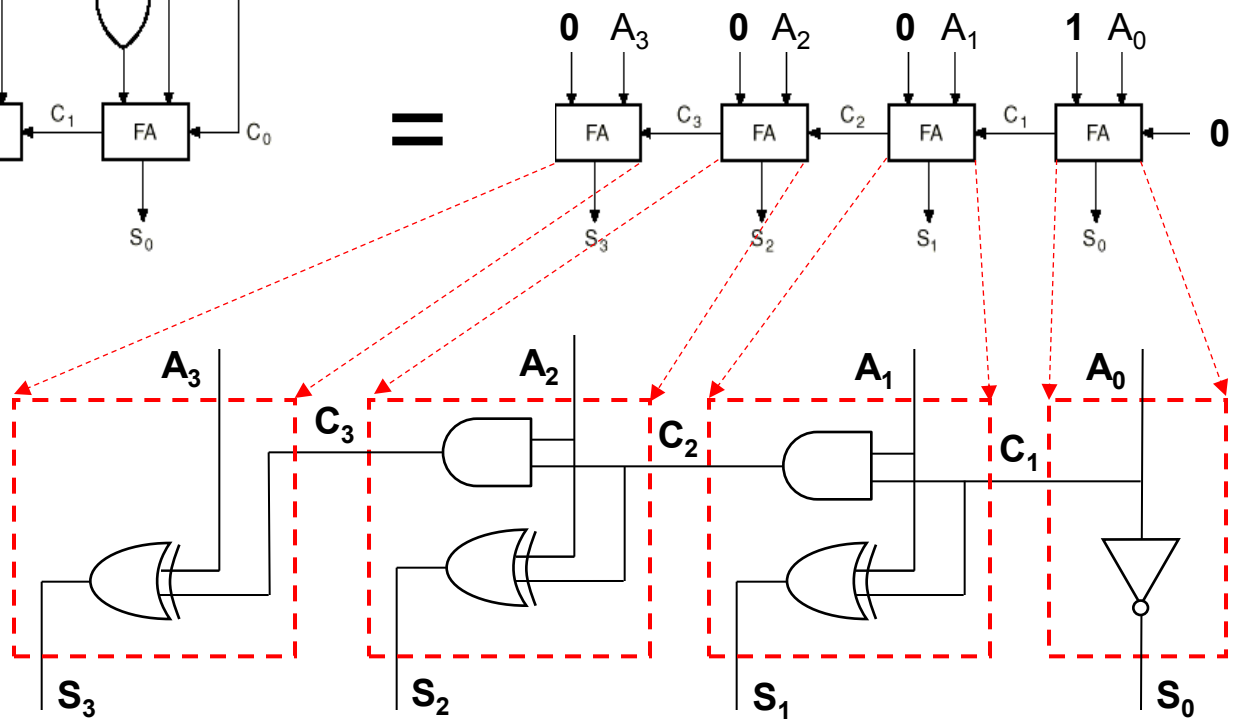
Increment by 1



$S_i = A_i \oplus B_i \oplus C_i$

$C_{i+1} = A_iB_i + A_iC_i + B_iC_i$

=



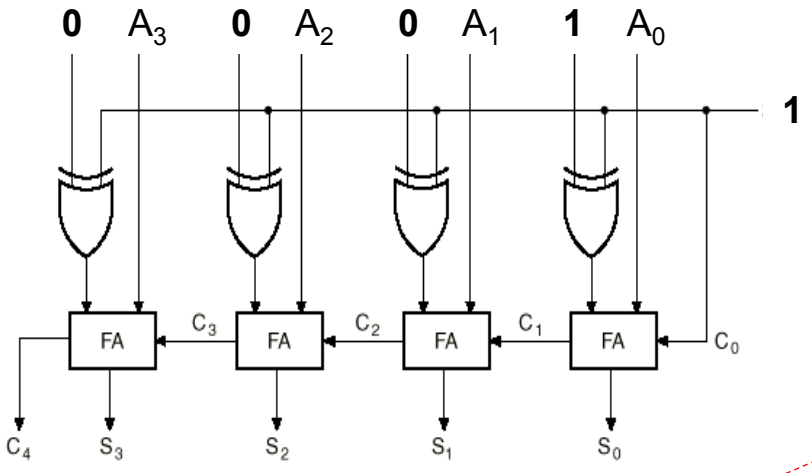
$S_{1,2,3} = A_i \oplus C_i$

$C_{2,3} = A_iC_i$

$S_0 = A_0'$

$C_1 = A_0$

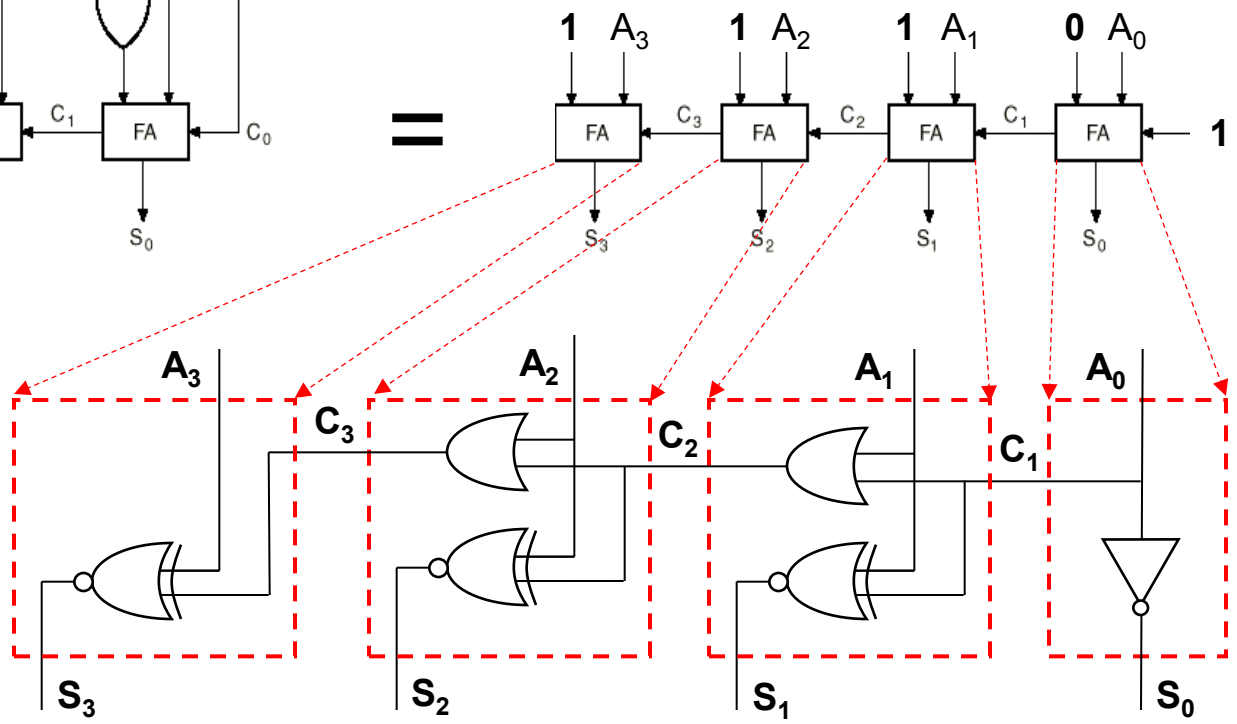
Decrement by 1



$S_i = A_i \oplus B_i \oplus C_i$

$C_{i+1} = A_iB_i + A_iC_i + B_iC_i$

=



$S_{1,2,3} = (A_i \oplus C_i)'$

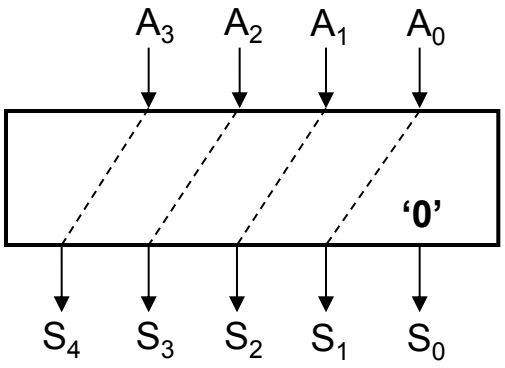
$C_{2,3} = A_i + C_i$

$S_0 = A_0'$

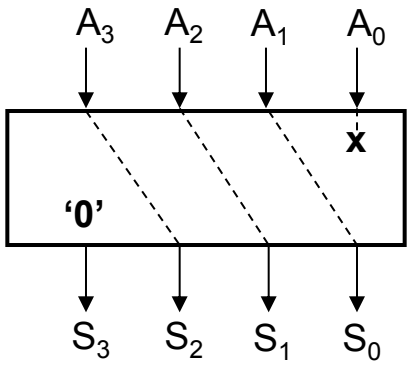
$C_1 = A_0$

Multiplication/Division by constant

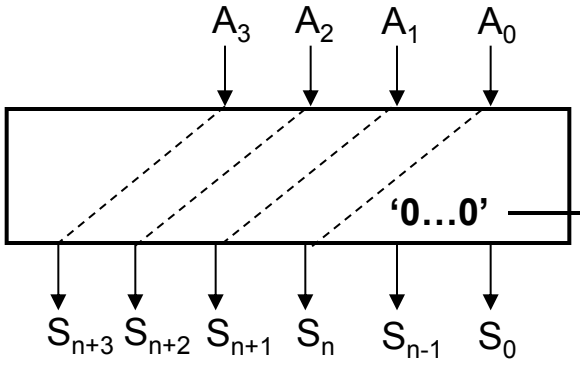
Multiplication by 2 (shift left)



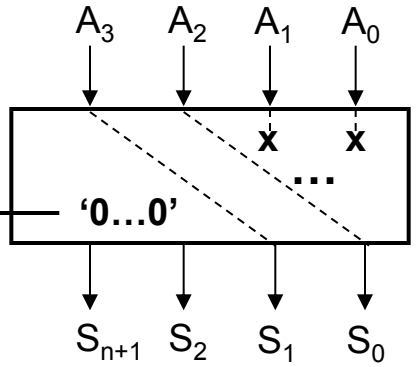
Division by 2 (shift right)



Multiplication by 2^n



Division by 2^n



n 'zeros'