Computer architecture
Homework week 1-2

Instructions
Submit by e-mail to the lecturer, as a PDF document with your name and student ID near the beginning. You can work in groups of 2. Deadline: Sept 12th, 23:59.

Question 1
Research and describe the x86 initialization sequence: what happens when the Pentium processor is powered up initially, until the operating system code starts to run. Phrase it in your own words: no copy-paste. Detail your information sources and explain why you trust them; do not source Wikipedia directly. Max 0,5 page A4.

Question 2
Research, define and separate the following concepts:

- throughput,
- bandwidth,
- latency,
- access time,
- performance,
- efficiency.

Again, phrase in your own words, one paragraph each. Explain the units in which these values are expressed, with examples. Max 1 page A4 in total.

Question 3
Explain why IPC and CPI are not simply inverse of each other. Use examples and/or analogies. Max 0.5 page A4.
**Question 4**

Find a single processor model that satisfies the following:
- manufactured any time between 1950 and 2010;
- not by Intel;
- not supporting Intel’s x86 instruction set natively.

Then write a small report that details the following:
- Year when first sold as product;
- Company selling the 1st product;
- What it was know to be good for (at the time, eg "it was the first with this feature" or "it was the fastest at the time", etc.);
- The name of some example software programs written for it (or running on it);
- Typical clock frequency;
- If known:
  - how many instructions it supported;
  - number of transistors on chip (eg. 25million);
  - Silicon die area (mm2, eg. 110mm2);
  - L1 and L2 cache size on chip (if applicable, eg. 32KB L1, 512KB L2);
  - Technology size (microns/nanometers, eg. 65nm)

Ensure that your report contains links to the sources of your information.
Max 1 page A4.

**Note**
The entire class will receive a bonus proportional to the number of different processors handled by the class a whole. So if everyone reports on the same processor there will be no bonus, if everyone reports on a different processor everyone will receive maximum extra credits.

Hint: the period 1970-1985, or microcontrollers.

**Question 5**

Suppose a 9% reduction in voltage results in a 9% reduction in frequency in a processor chip. What is the impact on dynamic power?

**Question 6**

A RISC core uses a 6-stage RISC pipeline (Fetch, Decode, Read, Execute, Memory, Writeback). At the current CMOS technology size, its L1 cache has an access time of 1.4ns.

Can you say something about the min/max frequency range of this core and why?
Question 7

Increasing the L1 cache size increases the access time to 2.1ns. To preserve the cycle time, another memory stage is added to the pipeline. How does this affect the startup time and half-performance vector length?